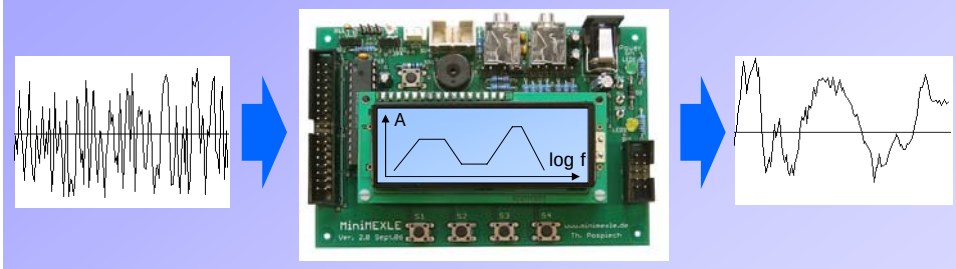
DSP on MiniMEXLE



Basics of Digital Signal Processing with AVR µCs

Overview

1. Introduction to DSP
2. Analog ←→ Digital
3. DSP Special Functions

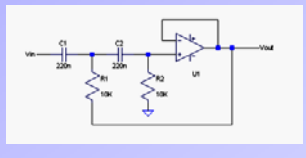
Overview (1)

1. Introduction to DSP
2. Analog ←→ Digital
3. DSP Special Functions

Why Digital Signal Processing?

Analog Signal Processing

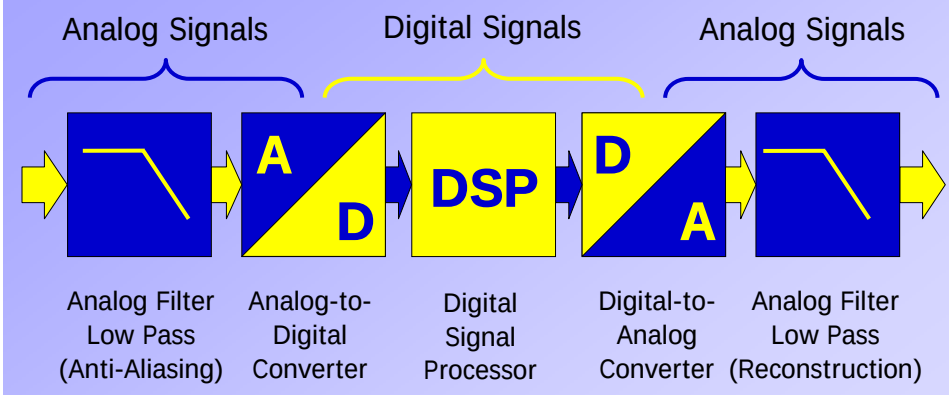
- Analog signals (voltage, current) represent value
- Component variation
- Temperature dependent
- Low integration scale
- Expensive and big
- Very limited functionality



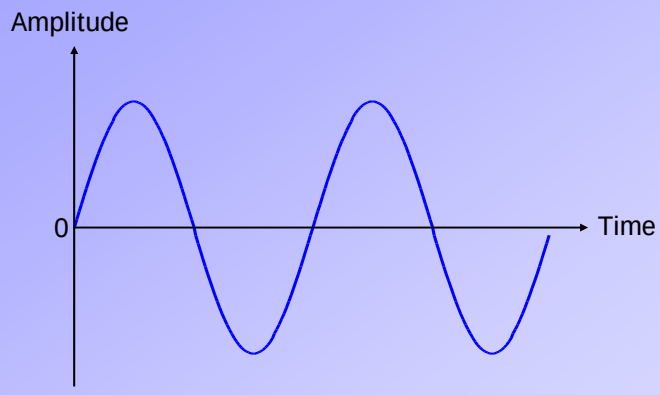
Digital Signal Processing

- Digital signals (logical signals) represent value
- Fixed logical function
- Temperature independent
- High integration scale
- Cheap and small
- Very complex functionality

DSP System Structure

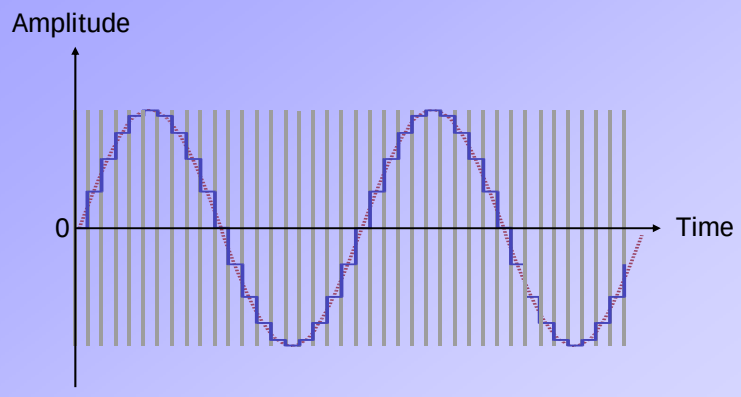


Continuous Signals



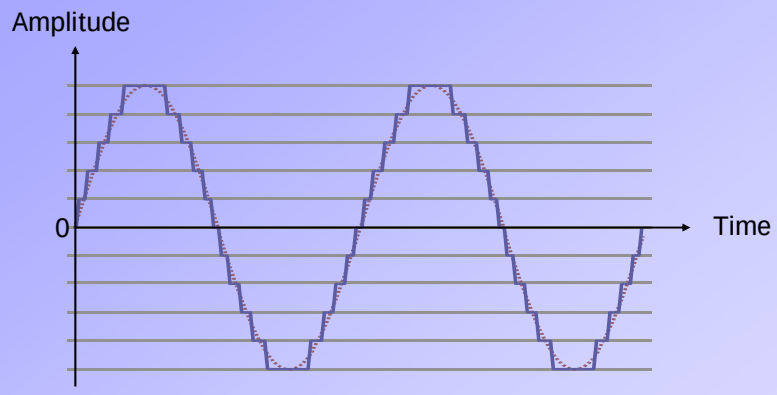
Continuous in amplitude and continuous in time

Time discrete Signals



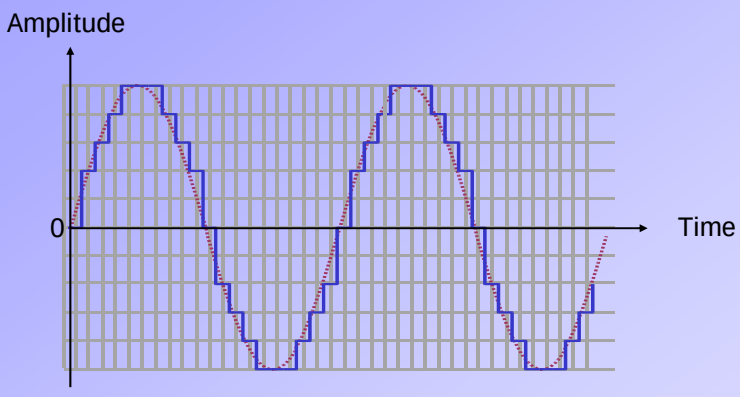
Continuous in amplitude and discrete in time

Quantized Signals



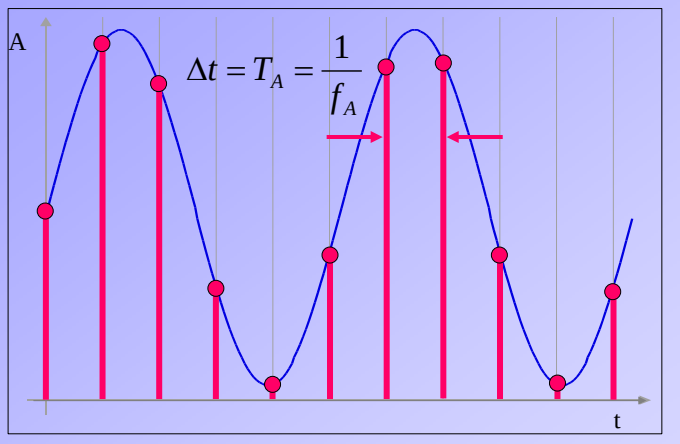
Discrete in amplitude and continuous in time

Digital Signals



Discrete in amplitude and discrete in time
➔ series of numbers

Sampling



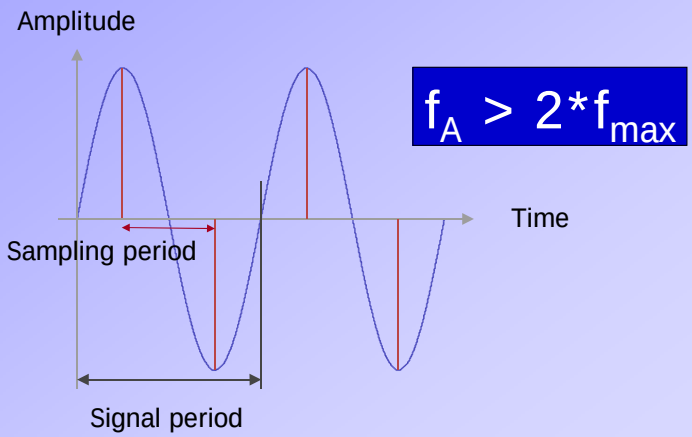
Sampling period T_A , Sampling frequency f_A (samples/s)

Standard Sampling Rates

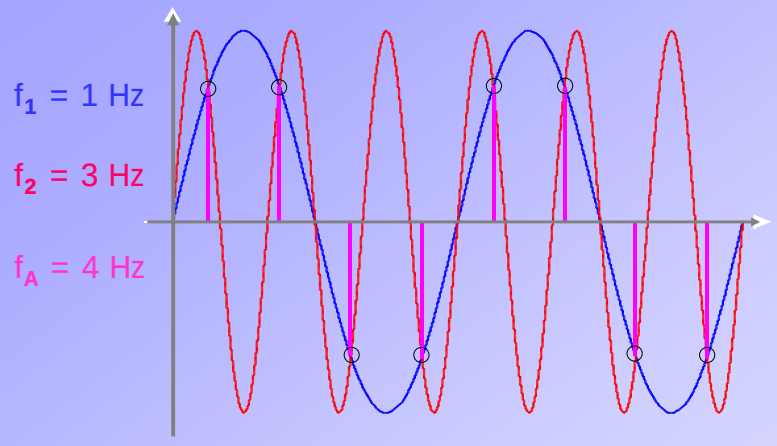
- ISDN (Integrated Services Digital Network) 8 kHz
- DSR (Digital Satellite Radio - Germany) 32 kHz
- Audio CD (Compact Disk) 44,1 kHz
- DAT (Digital Audio Tape) 48 kHz
- DVD-Audio 48 kHz
- DVD-Audio, Professional Recording 96 kHz
- Digital Video 11 MHz

Nyquist-Shannon Sampling Theorem

For Sinusoid signals we need minimum 2 samples/period



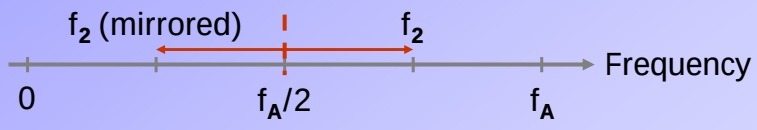
Subsampling



Identical values for both input frequencies f_1 and f_2
for $f_A - f_2 = f_1$ (mirroring)

Aliasing

Aliasing is the effect which happens during sampling when Nyquist-Shannon Sampling Theorem is not satisfied



Frequencies above $f_A/2$ are mirrored back to the frequency range from $f_A/2$ to 0.

Oversampling

Using much higher sampling frequency then needed by the request of Nyquist-Shannon Sampling Theorem

$$f_A = M * f_{Ny}$$

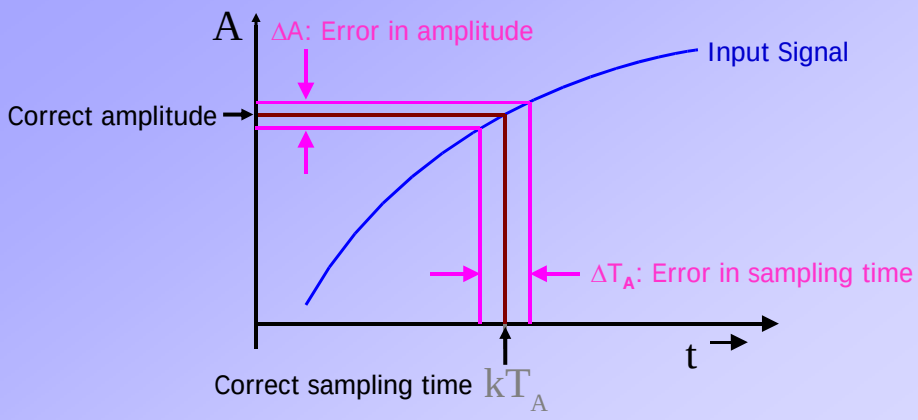
f_A = current sampling frequency

M = oversampling factor

f_{Ny} = minimum sampling frequency

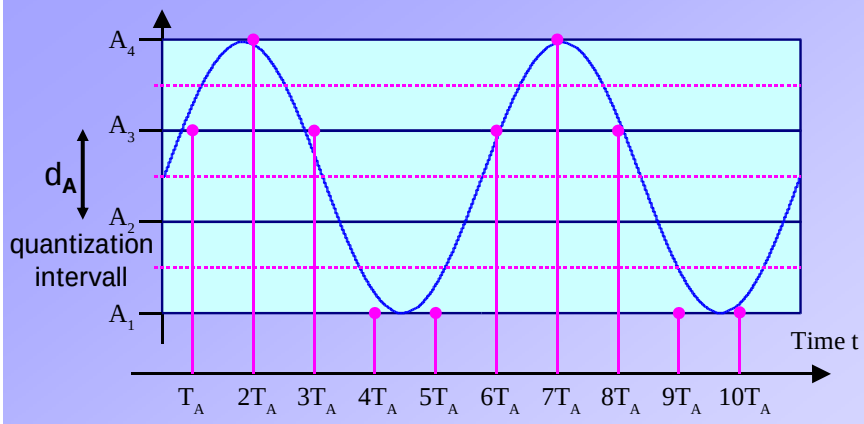
➔ Much more „relaxed“demands for the filters

Sampling error (Jitter)



Jitter error depends on gradient of input signal at sampling time

Quantization

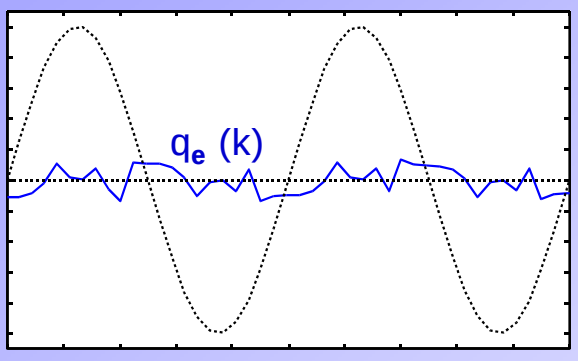


Quantization with 2 Bits ➔ 2^2 = 4 quantization levels

$N = 2^b$

N = quantization levels
b = number of bits

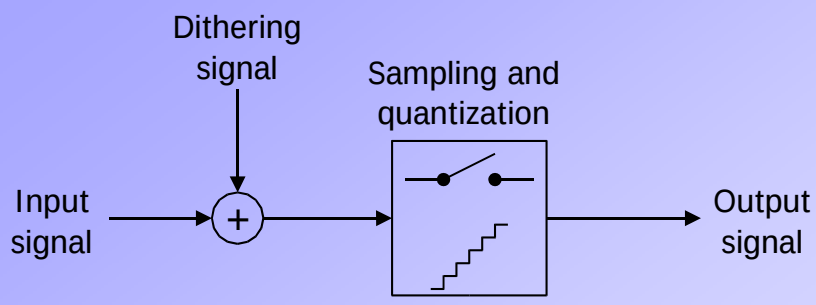
Quantization error



Quantization error $q_e(k)$is depending on input signal

Maximum error is ± 0,5 d (half of quantization interval)

Dithering



Dithering signal = “noise signal”, independent from input signal

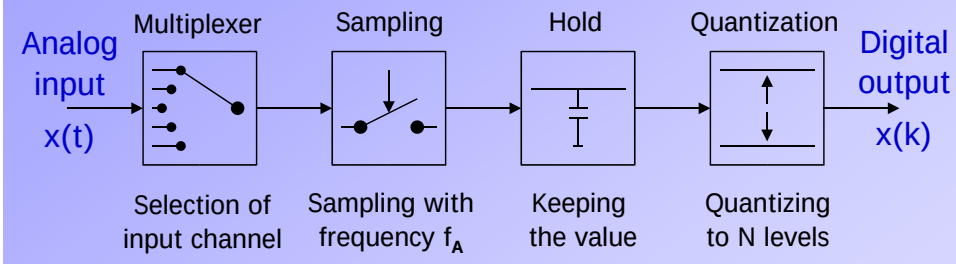
Reduces the dependency of quantization error from input signal

➔ Better “subjective quality” of output signal

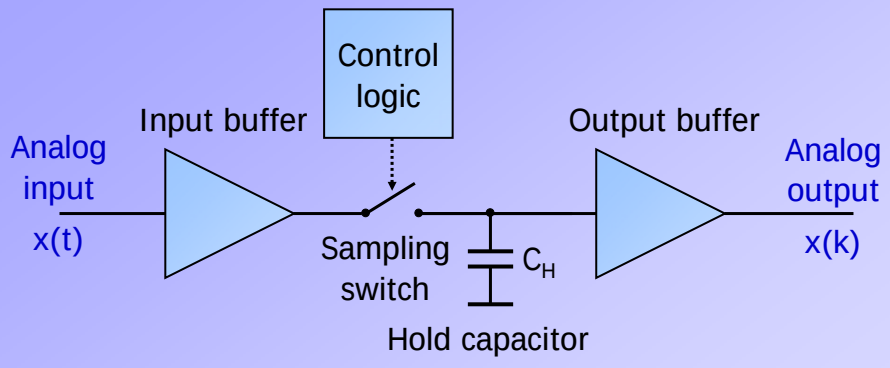
Overview (2)

1. Introduction to DSP
2. Analog ←→ Digital
3. DSP Special Functions

Analog-to-Digital Converters



Sample and Hold

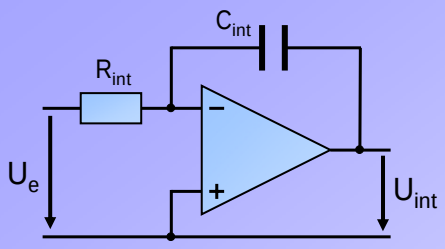


Sampling switch is closed only for very short time to charge C_H

Hold capacitor keeps the value during the AD-Conversion

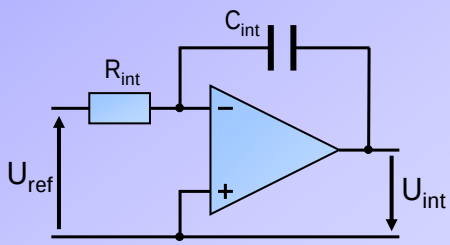
Integrating ADC

Integration period



$$U_{int} = U_0 + k_{int} t_{int} U_e$$

Deintegration period



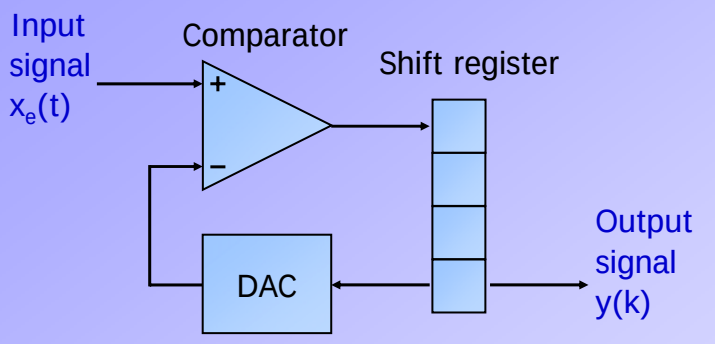
$$k_{int} t_{int} U_e - k_{int} t_{mess} U_{ref} = 0$$

$$t_{mess} = t_{int} \frac{U_e}{U_{ref}}$$

U_{int} = Output voltage of integrator
U_0 = Starting voltage (mostly = 0)
k_{int} = Time constant of integration
t_{int} = Fixed integration time
U_e = Input voltage

U_{ref} = Reference voltage (fixed)
t_{mess} = Measured deintegration time

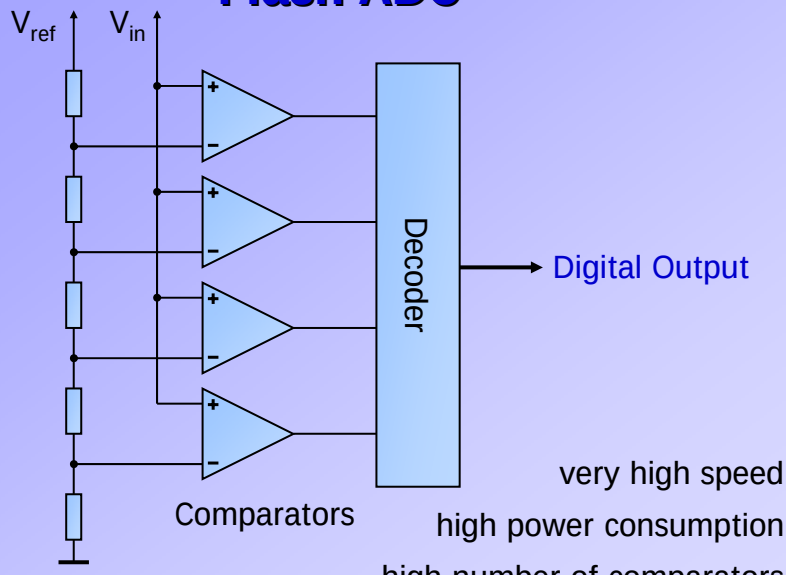
Successive Approximation ADC



Principle: Step-by-step comparison of digital output with analog input: Bits are evaluated from MSB to LSB.

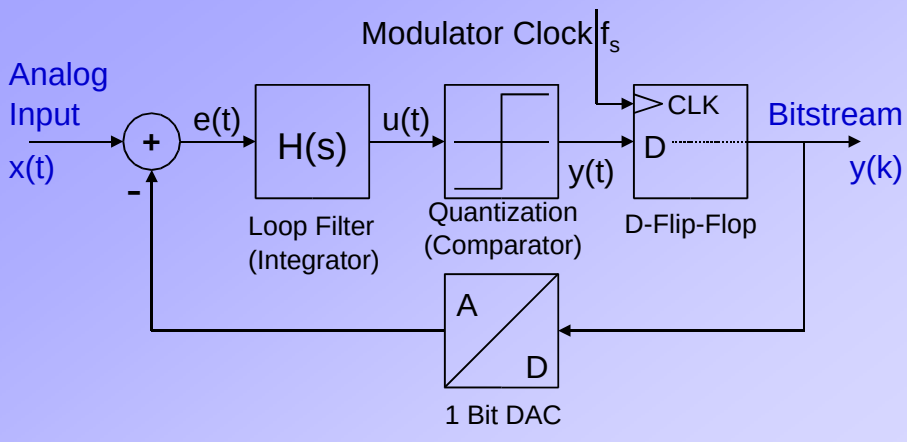
Needs N steps for N bits resolution.

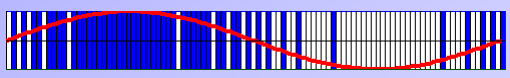
Flash ADC



very high speed
high power consumption
high number of comparators

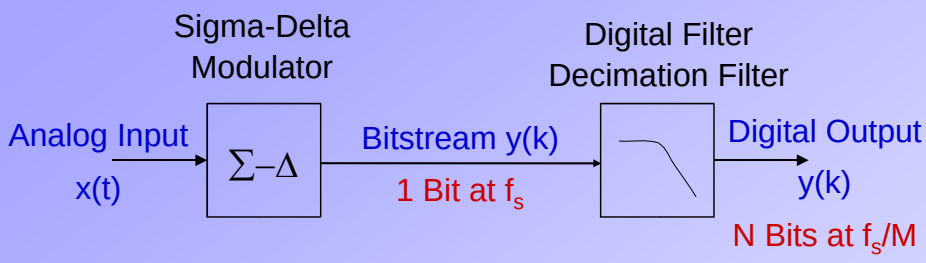
Sigma-Delta ADC (1)





Sigma-Delta Modulation is Pulse-Density-Modulation

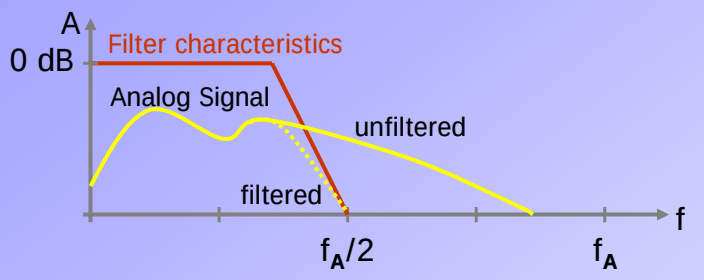
Sigma-Delta ADC (2)



Analog input signal is converted to a serial „Bitstream“.
The Bit-frequency used is in the range of 1-4 MHz.

The digital decimation filter creates a N-Bit resolution but at lower frequency (Low pass → Averaging)

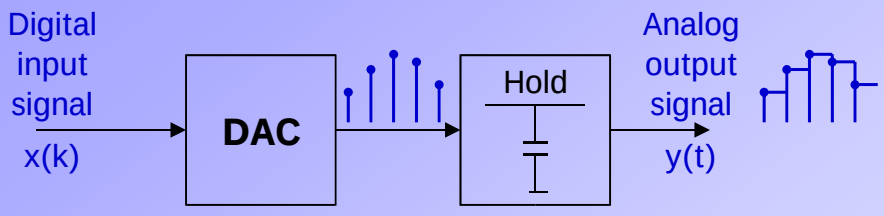
Anti-Alias Filter



Anti-Alias Filter suppresses input signal parts above $f_A/2$ to prevent the effect of “mirroring”.

The filter suppression at $f_A/2$ must fit to the ADC resolution. (Example: 10 Bit ADC → filter suppression at $f_A/2$ = - 60 dB

Digital-to-Analog Converters

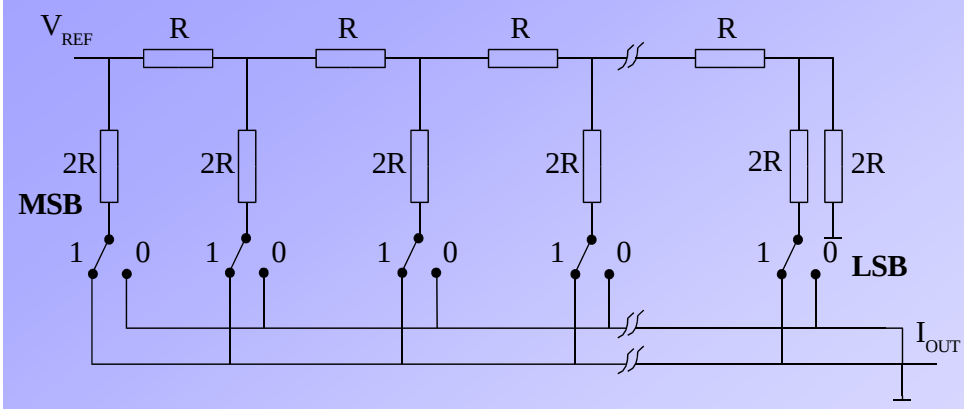


Digital input signal = series of number at sample frequency

DAC output signal = series of analog impulses

Analog output signal = time continuous analog signal

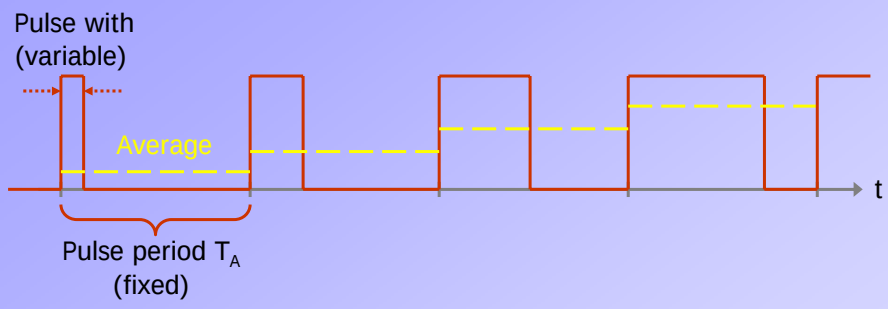
R-2R Ladder DAC



Every branch of the ladder has a division factor of 2

The output current I_{OUT} has therefore binary steps

Pulse-With-Modulator DAC

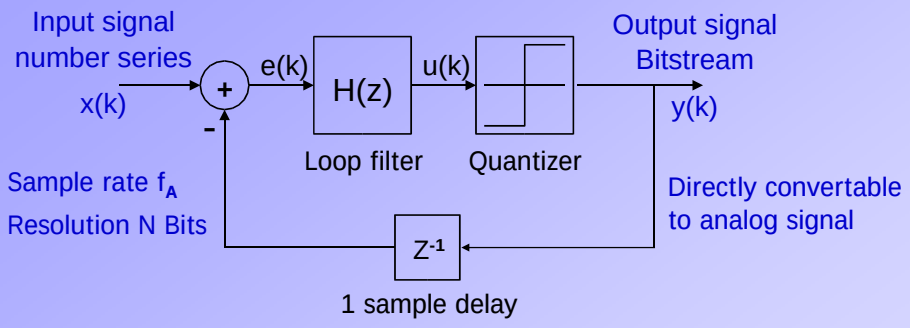


Discrete amplitudes transformed to proportional pulse with

Widely used in µC (on-chip peripheral) and for motor control

Non-linear effects for higher input frequencies

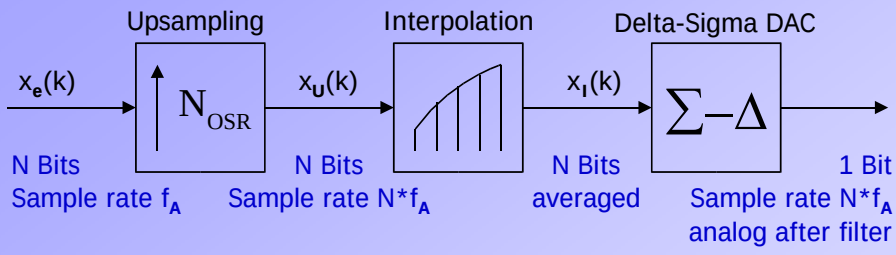
Delta-Sigma DAC (1)



Conversion of N Bits input series to 1 Bit bitstream.

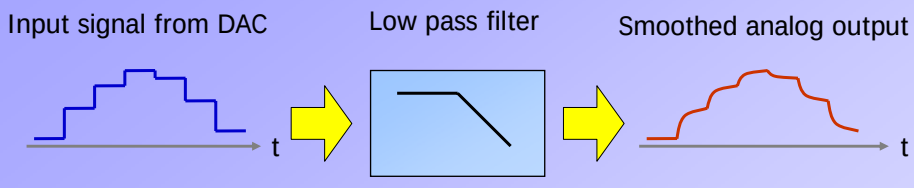
Bitstream after low pass filtering gives analog signal

Delta-Sigma DAC (2)



Widely used as high quality DAC e.g. for Audio signals
(1-Bit technology)

Reconstruction Filter

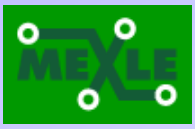


High frequencies of the „sharp“ steps are damped

Results in more smooth „sound“ at the filter output

Overview (3)

1. Introduction to DSP
2. Analog ←→ Digital
3. DSP Special Functions

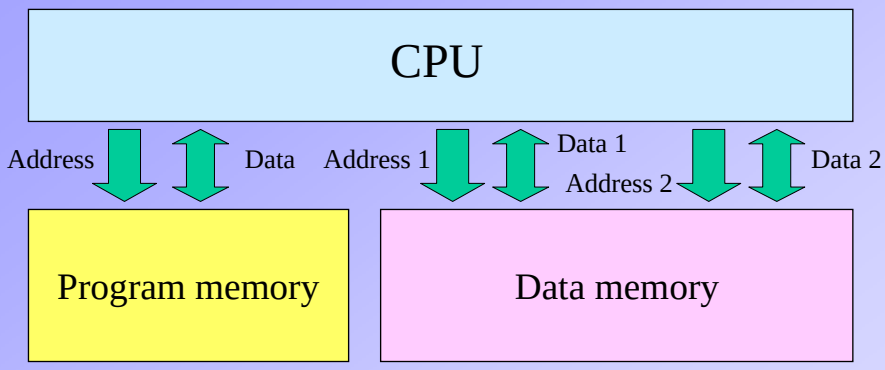


DSP Specialties

Demands to a processor optimized for Digital Signal Processing

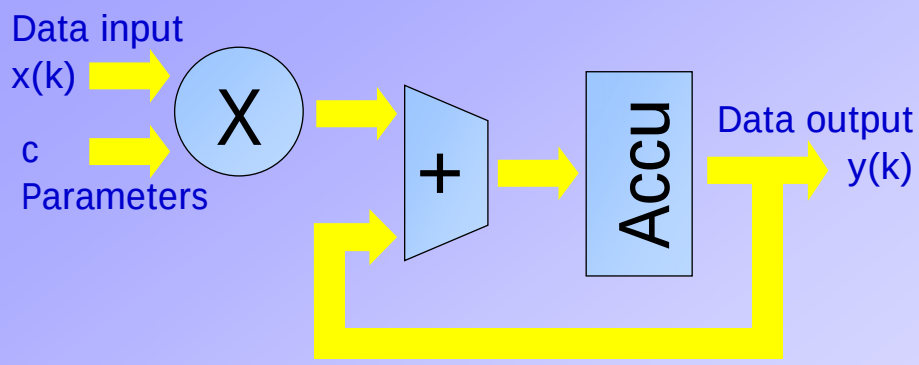
- ➔ to process a lot of complex mathematical operations in **optimal high calculation speed**
- ➔ to operate several tasks at the same time by **parallel functional units**
- ➔ to optimize the memory usage by **several pointers a**nd a **special address-ALU**
- ➔ to reduce electrical power consumption by **energy saving design**

Harvard Architecture



Separate program and data memory with separate buses ensure optimal fast parallel access to program, data and parameters

MAC-Unit

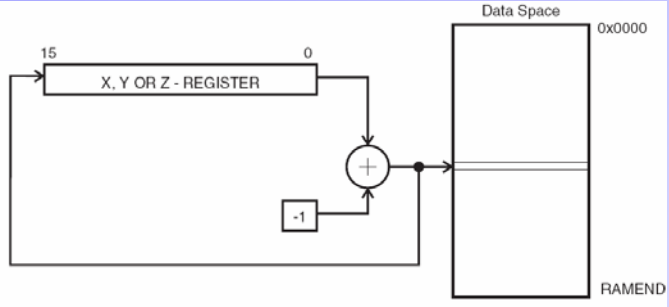


Combined unit for Multiplication, Addition and Accumulation suitable for digital filter calculations:

$$y(k) = c \bullet x + y(k-1)$$

Special Addressing Modes

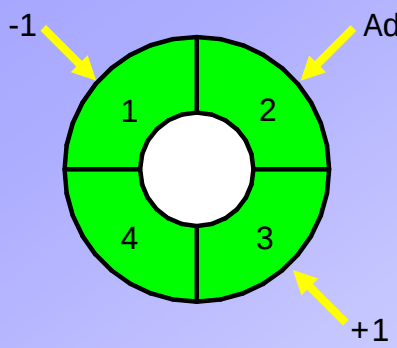
- Extended pointer addressing of data in memory with Pre/Post Increment/Decrement of pointers



- Ring Buffer structures
- Bit Reversal Addressing

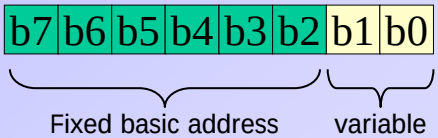
Ring Buffer

Closed ring of limited number of variable space (array)

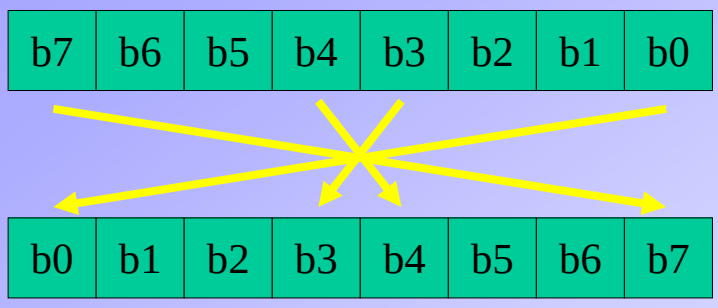


Realized by software

or by “Modulo Addressing”



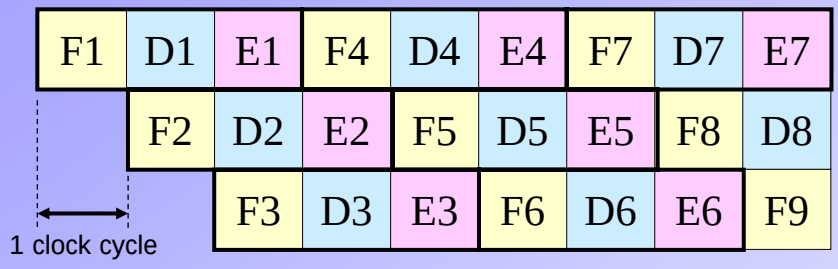
Bit Reversal Addressing



Exchange of bit positions

Needed for performing Fast Fourier Transform (FFT)

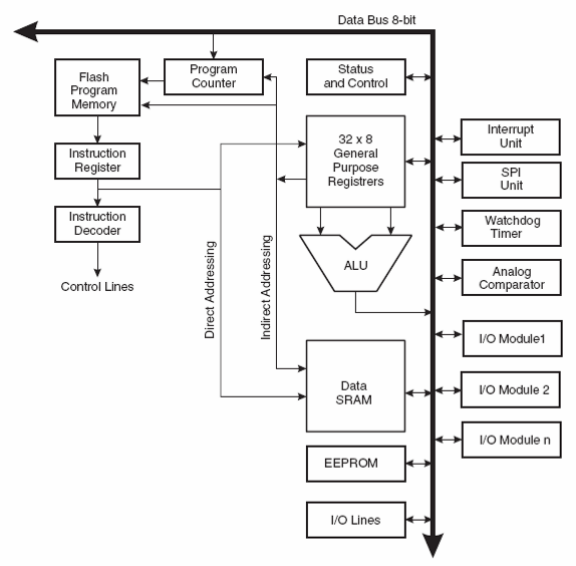
Pipelining



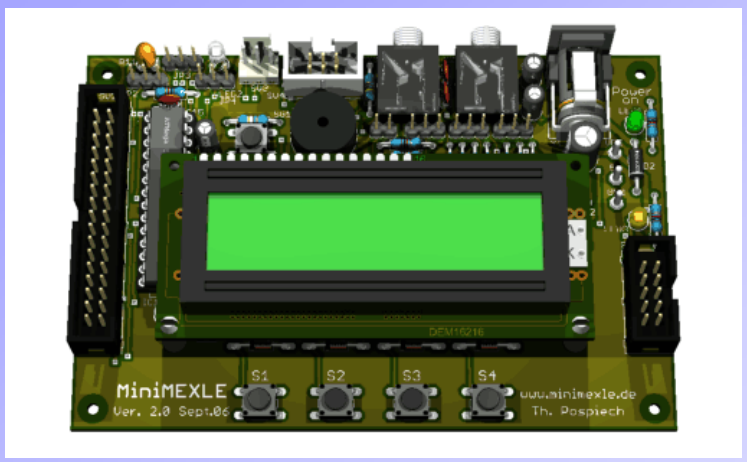
F = Fetch ; D = Decode ; E = Execute

Example of pipeline with 3 stages.
3 operations are processed quasi in parallel

DSP on Atmel AVR



- Harvard structure
- 2-cycle HW multiplier
- 20 MIPS at 20 MHz
- 131 instructions (most single cycle)
- Extended addressing modes (pointers)
- 32 x 8 Bit registers
- 10 Bit ADCs
- PWM-Output 8/16 Bit



Thank you very much for your attention